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lab 6

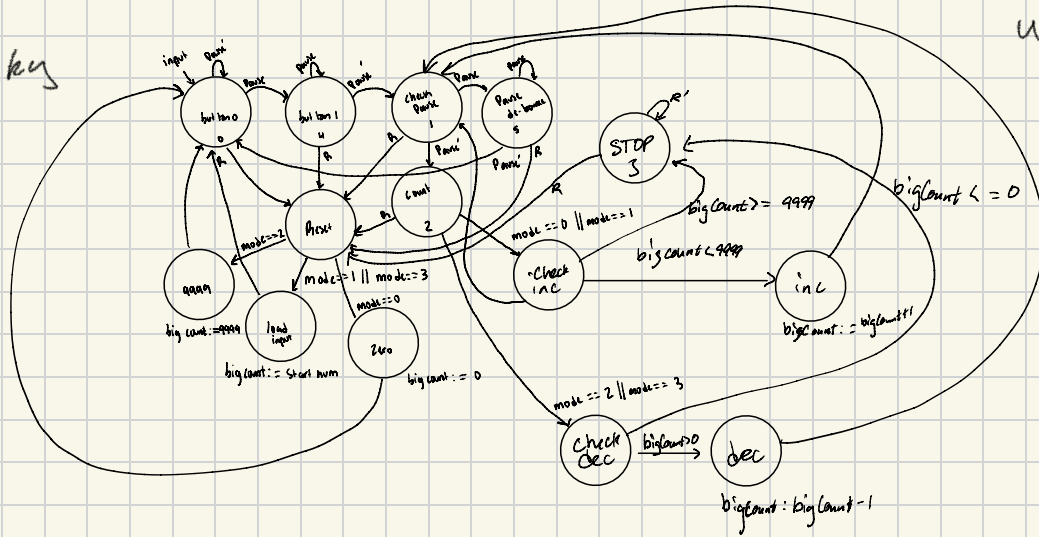
input mode bits (2'b), load (8'b), Preset (1'b), Pause (1'b), Start num (4'b)

output ms1 (4'b), ms10 (4'b), s1 (4'b), s10 (4'b)

local storage state (2b), next state (2b), big count (14'b)

(input clock for this has 6ns period)
(meaning 2 state transitions every 10ns)

up-counter HLSM

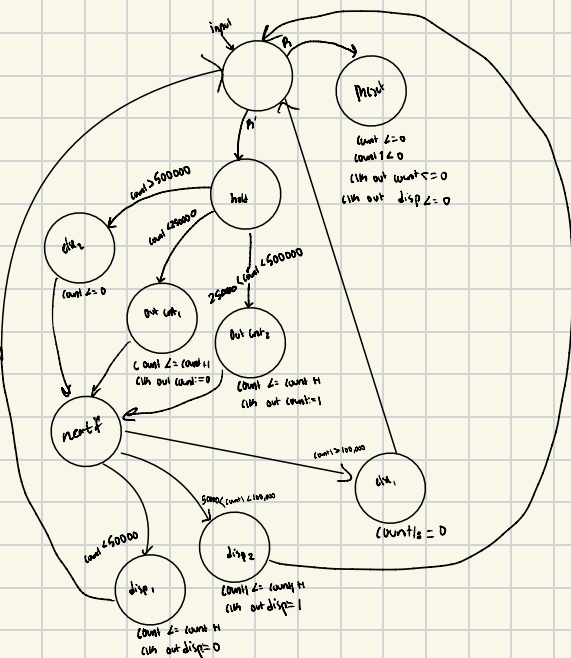


clkdiv HLSM

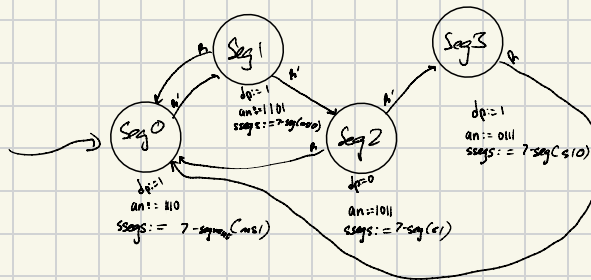
inputs: Preset

Output: clk out count, clk out disp

local storage: count (20'b), count1 (17'b)



Seven-Segment HLSM

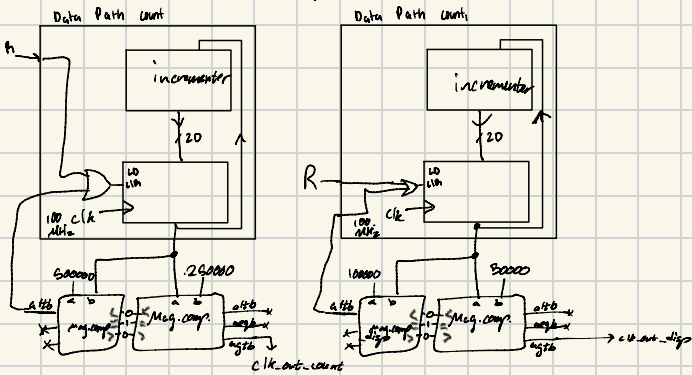


inputs ms1 (4'b), ms10 (4'b), s1 (4'b), s10 (4'b)

outputs an (4'b), ssegs (7'b), dp

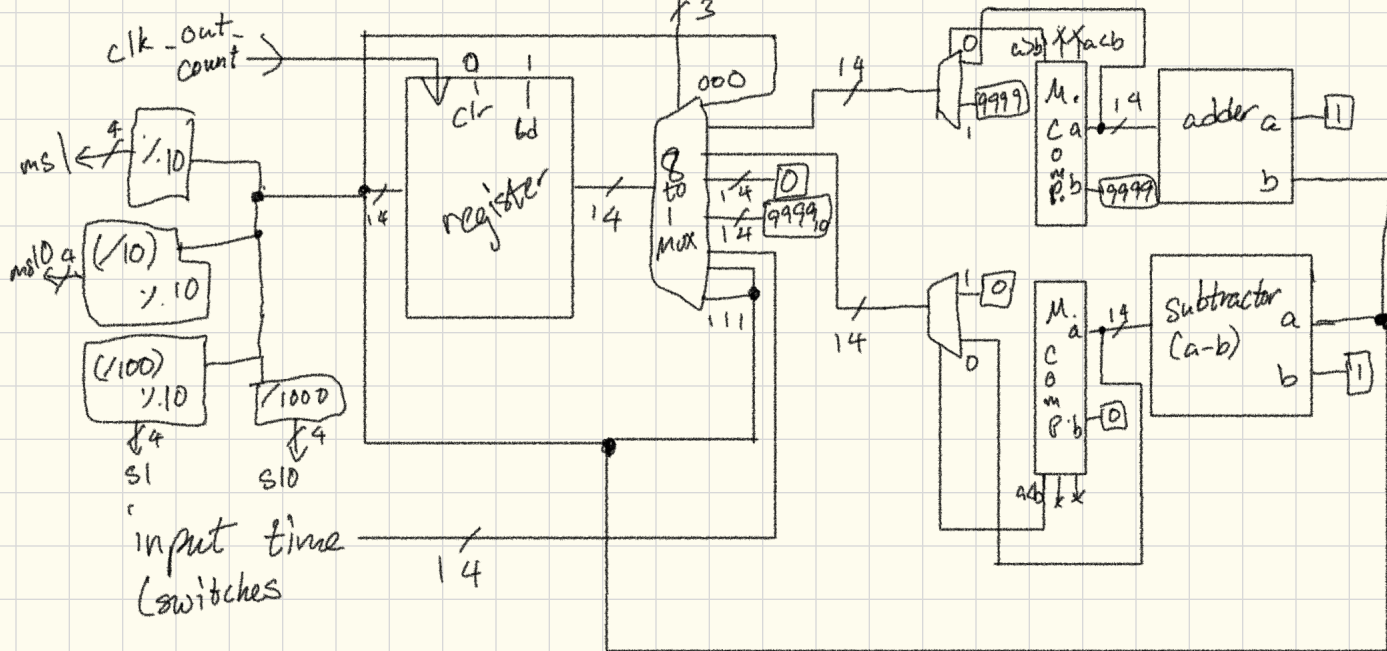
7-segment (4'b input) returns the 7-segment value for these digits.

clkdiv datapaths



input clock: clk_out_count

Up-Counter



Data path

7-segment

controller (input clock: clk_out_disp)

